CLAIMS

What is claimed is:

1. An ultra-thin semiconductor package device comprising:

a lead frame comprising a die pad, a plurality of leads disposed around the die pad, and tie bars connected to and disposed around the die pad, wherein said die pad comprises a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip mounted to the die pad chip attaching part, said chip having a plurality of electrode pads, wherein the plurality of electrode pads are electrically interconnected to the leads, and wherein each of the leads comprises integrally connected inner leads and outer leads;

an encapsulant encapsulating the semiconductor chip to form a package body, wherein said inner leads are encapsulated by the encapsulant and said outer leads are external to the encapsulant; and

said chip attaching part having a first thickness and the inner leads having a second thickness greater than the first thickness.

2. An ultra-thin semiconductor package device according to claim 1, wherein the first thickness is between about 30% to 50% of the second thickness.

3. An ultra-thin semiconductor package device according to claim 1, wherein the chip attaching part and the peripheral part have the same thickness.

4. An ultra-thin semiconductor package device according to claim 1 further comprising two semiconductor chips each attached to a corresponding side of the die pad chip attaching part.

5. An ultra-thin semiconductor package device according to claim 1, wherein the die pad is located below the leads.

6. An ultra-thin semiconductor package according to claim 1, wherein the plurality of electrode pads are electrically interconnected to the leads via bonding wires, and wherein the bonding wires are connected by balls formed on the surface of the leads and stitches formed on the electrode pads.

7. An ultra-thin semiconductor package device according to claim 6, wherein metal bumps are formed on the electrode pads of the chip and the stitches are formed on the metal bumps.

8. An ultra-thin semiconductor package device according to claim 1, wherein upper and lower portions of the package body with reference to the leads have different thickness each other.

9. An ultra-thin semiconductor package device according to claim 5, wherein the tie bar has the same thickness as the leads.

10. An ultra-thin semiconductor package device according to claim 1, wherein the tie bar has the same thickness as the die pad peripheral part.

11. An ultra-thin semiconductor package device according to claim 1, wherein the peripheral part protrudes in both vertical directions from the chip attaching part, and the thickness of the peripheral part is equal to the thickness of the leads.

12. An ultra-thin semiconductor package device according to claim 1, wherein the die pad comprises divided first and second die pads.

13. An ultra-thin semiconductor package device according to claim 12, wherein the first and second die pads each include a chip attaching part and a peripheral part.

14. An ultra-thin semiconductor package device according to claim 1, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

15. An ultra-thin semiconductor package device according to claim 6, wherein the lead frame is made of iron-nickel alloy or copper alloy, and wherein the bonding wires are gold wires.

16. An ultra-thin semiconductor package device according to claim 1, wherein the semiconductor chip is a memory device and wherein the adhesive is a film-type adhesive tape made of an epoxy resin.

17. An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, and wherein the peripheral part has a thickness equal to the second thickness of the inner leads.

18. An ultra-thin semiconductor package device according to claim 17, wherein the die pad peripheral part protrudes toward the first semiconductor chip.

19. An ultra-thin semiconductor package device according to claim 18, wherein the package body has an upper thickness different from a lower thickness thereof, when viewed with reference to the leads.

20. An ultra-thin semiconductor package device according to claim 17, wherein the peripheral part protrudes toward the second semiconductor chip.

21. An ultra-thin semiconductor package device according to claim 20, wherein the die pad is disposed below the leads.

22. An ultra-thin semiconductor package device according to claim 17, wherein the bonding wires connected to one of the semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. An ultra-thin semiconductor package device according to claim 17, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

24. An ultra-thin semiconductor package device according to claim 23, wherein metal bumps are formed on the electrode pads and wherein the stitches are formed on the metal bumps.

25. An ultra-thin semiconductor package device according to claim 17, wherein the die pad comprises divided first and second die pads.

26. An ultra-thin semiconductor package device according to claim 25, wherein the first and second die pads each include a corresponding chip attaching part and a corresponding peripheral part.

27. An ultra-thin semiconductor package device according to claim 17, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. An ultra-thin semiconductor package device according to claim 17, wherein a thickness of the package body is about 580 μm, a thickness of the die pad peripheral part is about 100 μm, and a thickness of the chip attaching part is about 40 μm.

29. An ultra-thin semiconductor package device according to claim 17, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

30. A method of manufacturing an ultra-thin semiconductor package device, said method comprising:

preparing a lead frame comprising a die pad, a tie bar connected to and supporting the die pad, and a plurality of leads disposed around the die pad;

defining a chip attaching part and a peripheral part on the die pad, said peripheral part surrounding the chip attaching part;

etching the chip attaching part so that the chip attaching part has a thickness less than a thickness of the leads;

die bonding a semiconductor chip to the chip attaching part of the die pad;

wire bonding the semiconductor chip to the leads; and

forming a package body by encapsulating the semiconductor chip, bonding wires, and a portion of the leads.

31. A method according to claim 30, wherein the thickness of the chip attaching part is between 30-50% of the thickness of the leads.

32. A method according to claim 30, wherein the die pad peripheral part and the tie bar have the same thickness as the chip attaching part.

33. A method according to claim 30, wherein the die pad peripheral part and the tie bar each have a thickness equal to the thickness of the leads.

34. A method according to claim 33, wherein the die pad peripheral part protrudes upwardly and downwardly from the chip attaching part.

35. A method according to claim 33, wherein the die pad peripheral part protrudes in a single vertical direction from the chip attaching part.

36. A method according to claim 35, wherein the die pad is disposed below the leads.

37. A method according to claim 30, wherein an upper portion of the package body has a thickness different than a thickness of a lower portion of the package body.

38. A method according to claim 30, further comprising:

preparing a wafer having a plurality of semiconductor chips formed on an active surface of the wafer;

attaching an adhesive layer to the backside of the semiconductor chips and attaching a UV tape to the adhesive layer;

irradiating the UV tape with UV light to remove the adhesiveness between the UV tape and the adhesive layer;

cutting the wafer into the plurality of semiconductor chips; and

removing the plurality of semiconductor chips from the wafer state UV tape, wherein the adhesive layer remains attached to the backside of the chips, and wherein said die bonding attaches the chips to the chip attaching part using the adhesive layer.

39. A method according to claim 30, wherein the semiconductor chip comprises a first chip attached to a top surface of the chip attaching part and a second chip attached to a bottom surface of the chip attaching part, and wherein said die bonding comprises a first die bonding step for bonding the first chip and a second die bonding step for bonding the second chip.

40. A method according to claim 30, wherein the semiconductor chip comprises a first chip attached to a top surface of the chip attaching part and a second chip attached to a bottom surface of the chip attaching part, and wherein wire bonding comprises a first wire bonding step for electrically interconnecting the first chip to the leads and a second wire bonding step for electrically interconnecting the second chip to the leads.

41. A method according to claim 30, wherein the bonding wires are connected by balls formed on surfaces of the leads and stitches formed on the electrode pads.

42. A method according to claim 35, wherein bonding wires connected to one of the chips have different lengths from the bonding wires connected to the other chip.

43. A method according to claim 36, wherein the package body has a balanced structure with reference to the semiconductor chips.

44. A method according to claim 38, wherein the wafer preparation step comprises:

attaching a UV tape to the active surface of the semiconductor chip;

grinding a backside opposite to the active surface of the semiconductor chip;

irradiating the UV tape attached to the active surface with UV light; and

removing the UV tape from the active surface of the semiconductor chip.

45. A method according to claim 30, wherein forming the package body comprises injecting a mold resin in a temperature environment ranging between about 170 and 175 °C.

46. A method according to claim 38, wherein the adhesive layer comprises an epoxy resin.

47. A method according to claim 46, wherein the adhesive layer comprises a hardener made of amine.

48. A method according to claim 46, wherein the adhesive layer comprises a coupling agent made of silane.

49. A method according to claim 30, wherein the amount of etching is determined by a pressure and an applying time of an etchant.

50. An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, wherein said die pad includes a chip attaching part and a peripheral part surrounding the chip attaching part;

a semiconductor chip having a plurality of electrode pads formed on an active surface of the chip, said chip connected to the chip attaching part;

a package body for encapsulating the semiconductor chip;

bonding wires encapsulated by the package body, said bonding wires configured to electrically connect the electrode pads of the semiconductor chip to the leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body; and

wherein the chip attaching part has a first thickness and the inner lead has a second thickness that is greater than the first thickness.

51. An electronic apparatus according to claim 50, wherein the electronic apparatus is a memory card.

52. An electronic apparatus including a semiconductor package device having a package body of less than 0.7 mm of thickness, said semiconductor package device comprising:

a lead frame including a die pad, a plurality of leads disposed around the die pad, and a tie bar disposed around and connected to the die pad, said die pad including a chip attaching part and a peripheral part surrounding the chip attaching part, said peripheral part protruding away from the chip attaching part;

first and second semiconductor chips each having a plurality of electrode pads formed on an active surface of the chip, said first chip being attached to a top surface of the chip attaching part and the second chip being attached to a bottom surface of the chip attaching part;

a package body for encapsulating the semiconductor chip; and

bonding wires encapsulated by the package body and configured to electrically connect the electrode pads of the semiconductor chip and the plurality of leads, wherein each of the plurality of leads comprises an inner lead bonded to the bonding wire and encapsulated by the package body and an outer lead integral to the inner leads and extending from the package body, wherein said chip attaching part has a first thickness and the inner lead has a second thickness greater than the first thickness and equal to a thickness of the peripheral part.

53. An electronic apparatus according to claim 52, wherein the electronic apparatus is a memory card.